QUAD/DUAL EPAD® PRECISION MATCHED PAIR N-CHANNEL MOSFET ARRAY

FEATURES

- Electrically Programmable Analog Device CMOS Technology
- Operates from 2V, 3V, 5V to 10V
- Flexible basic circuit building block and design element
- Very high resolution -- average e-trim voltage resolution of 0.1mV
- Wide dynamic range -- current levels from 0.1μA to 3000μA
- Voltage adjustment range from 1.000V to 3.000V in 0.1mV steps
- Proven, non-volatile CMOS technology
- Typical 10 years drift of less than 2mV
- Usable in voltage mode or current mode
- High input impedance -- $10^{12}\Omega$
- Very high DC current gain -- greater than 10^9
- Device operating current has positive temperature coefficient range and negative temperature coefficient range with cross-over zero temperature coefficient current level at 68μA
- Tight matching and tracking of on-resistance between different devices with e-trim
- Wide dynamic resistance matching range
- Very low input currents and leakage currents
- Low cost, monolithic technology
- Application-specific or in-system programming modes
- Optional user software-controlled automation
- Optional e-trim of any standard/custom configuration
- Micropower operation
- Available in standard PDIP, SOIC and hermetic CDIP packages
- Suitable for matched-pair balanced circuit configuration
- Suitable for both coarse and fine trimming as well as matched MOSFET array applications

BENEFITS

- Precision matched electrically after packaging
- Simple, elegant single-chip user option to trimming voltage/current values
- Excellent device matching characteristics with or without additional electrical trim
- Remotely and electrically trim parameters on circuits that are physically inaccessible
- Usable in environmentally sealed circuits
- No mechanical moving parts -- high G-shock tolerance
- Improved reliability, dependability, dust and moisture resistance
- Cost and labor savings
- Small footprint for high board density applications

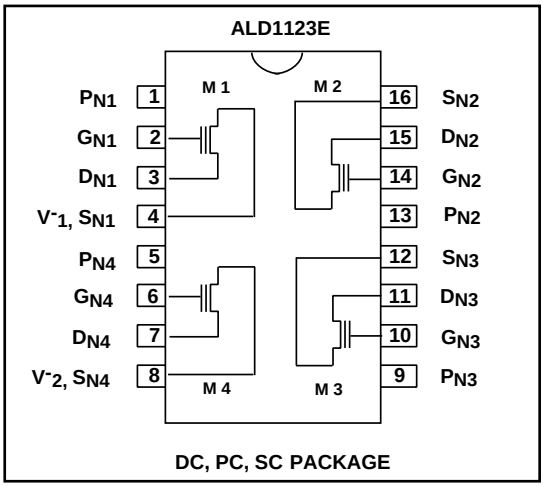
ORDERING INFORMATION

Operating Temperature Range*		
	0°C to +70°C	0°C to +70°C
	16-Pin Plastic Dip Package	16-Pin SOIC Package
	ALD1123E PC	ALD1123E SC

Operating Temperature Range*		
	0°C to +70°C	0°C to +70°C
	8-Pin Plastic Dip Package	8-Pin SOIC Package
	ALD1121E PA	ALD1121E SA

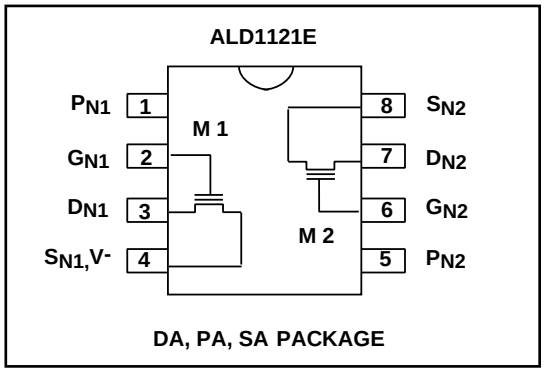
* Contact factory for industrial temperature range

PIN CONFIGURATION



DC, PC, SC PACKAGE

PIN CONFIGURATION

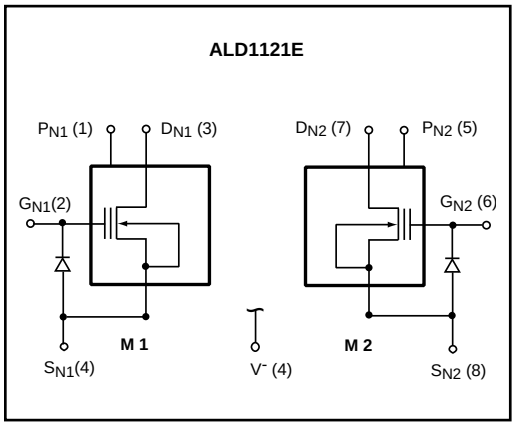


DA, PA, SA PACKAGE

APPLICATIONS

- Precision PC-based electronic calibration
- Automated voltage trimming or setting
- Remote voltage or current adjustment of inaccessible nodes
- PCMCIA based instrumentation trimming
- Electrically adjusted resistive load
- Temperature compensated current sources and current mirrors
- Electrically trimmed/calibrated current sources
- Permanent precision preset voltage level shifter
- Low temperature coefficient voltage and/or current bias circuits
- Multiple preset voltage bias circuits
- Multiple channel resistor pull-up or pull-down circuits
- Microprocessor based process control systems
- Portable data acquisition systems
- Battery operated terminals and instruments
- Remote telemetry systems
- E-trim gain amplifiers
- Low level signal conditioning
- Sensor and transducer bias currents
- Neural networks

BLOCK DIAGRAM



GENERAL DESCRIPTION

ALD1123E/ALD1121E are monolithic quad/dual EPAD® (Electrically Programmable Analog Device) N-channel MOSFETs with electrically adjustable threshold (turn-on) voltage. The ALD1123E/ALD1121E are precision matched and adjusted (e-trimmed) at the factory resulting in quad/dual MOSFETs that are highly matched in electrical characteristics. The ALD1123E has four (4) separate source pins. SN1, SN2 share a common substrate pin V-1 which has to be connected to the most negative voltage potential. Likewise, SN3, SN4 share a common substrate pin V-2 which has to be connected to the negative voltage potential for SN3, SN4. The ALD1121E has two (2) separate source pins (SN1, SN2). Both SN1, SN2 share a common substrate pin 4 which has to be connected to the most negative voltage potential.

Using an ALD1123E/ALD1121E MOSFET array is simple and straight forward. The MOSFETs function in electrical characteristics as n-channel MOSFETs except that all the devices have exceptional matching to each other. For a given input voltage, the threshold voltage of a MOSFET device determines its drain on-current, resulting in an on-resistance characteristic that can be precisely preset and then controlled by the input voltage very accurately. Since these devices are on the same monolithic chip, they also exhibit excellent tempco matching characteristics.

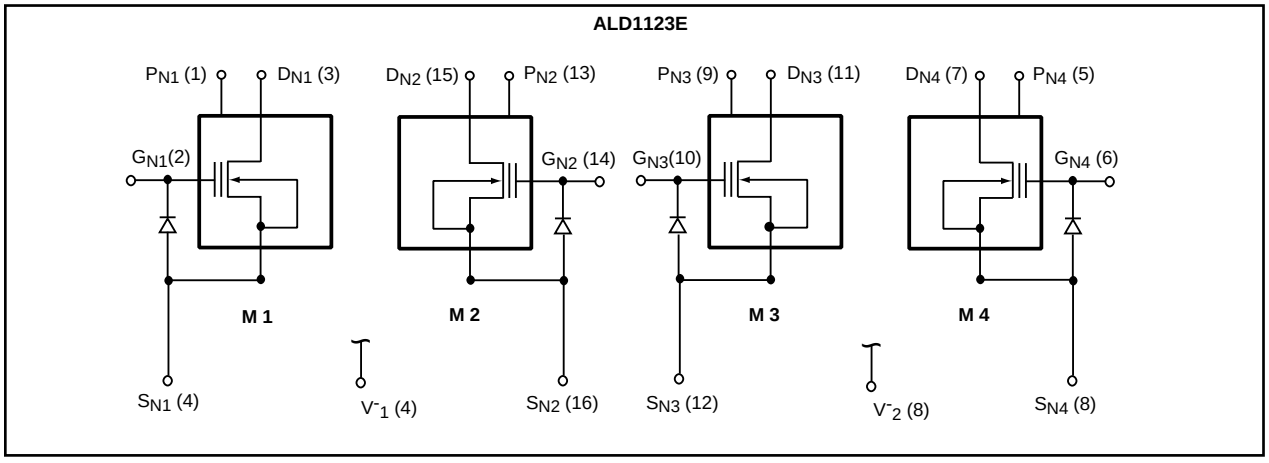
These MOSFET devices have very low input currents, and as a result a very high input impedance (>10^{12} Ohm). The gate voltage from a control source can drive many MOSFET inputs with practically no loading effects. Used in precision current mirror or current multiplier applications, they can be used to provide a current source over a 100 nA to 3 mA range, and with either a positive, negative or zero tempco.

Optional EPAD Threshold Voltage Trimming By User

The basic EPAD MOSFET device is a monotonically adjustable device which means the device can normally be e-trimmed to increase in threshold voltage and to decrease in drain-on current as a function of a given input bias voltage. Used as an in-circuit element for trimming or setting a combination of voltage and/or current characteristics, it can be e-trimmed remotely and automatically. Once e-trimmed, the set voltage and current levels are stored indefinitely inside the device as a nonvolatile stored charge, which is not affected during normal operation of the device, even when power is turned off. A given EPAD device can be adjusted many times to continually increase its threshold voltage. A pair of EPAD devices can also be connected differentially such that one device is used to adjust a parameter in one direction and the other device is used to adjust the same parameter in the other direction.

The ALD1123E/ALD1121E can be e-trimmed with the ALD EPAD programmer to obtain the desired voltage and current levels. Or they can be e-trimmed as an active in-system element in a user system, via user designed interface circuitry. PN1, PN2, etc., are pins required for optional e-trim of respective MOSFET devices. If unused, these pins are to be connected to V- or ground. For more information, see Application Note AN1108.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply voltage, V^+ referenced to V^- ——— -0.3V to +13.2V
Supply voltage, V_S referenced to V^- ——— ±6.6V
Differential input voltage range ——— 0.3V to V^+ +0.3V
Power dissipation ——— 600 mW
Operating temperature range PA, SA, PC, SC package ——— 0°C to +70°C
DA, DC package ——— -55°C to +125°C
Storage temperature range ——— -65°C to +150°C
Lead temperature, 10 seconds ——— +260°C

OPERATING ELECTRICAL CHARACTERISTICS
T_A = 25°C V^+ = +5.0V unless otherwise specified

Parameter	Symbol	ALD1123E Min	ALD1123E Typ	ALD1123E Max	ALD1121E Min	ALD1121E Typ	ALD1121E Max	Unit	Test Conditions
Drain to Source Voltage [1]	V_{DS}			10.0			10.0	V	
Initial Threshold Voltage [2]	V_{ti}	0.990	1.000	1.010	0.990	1.000	1.010	V	I_{DS} = 1µA T_A = 21°C
E-trim Vt Range	V_t	1.000		3.000	1.000		3.000	V	
Drain - Gate Connected Voltage Tempco	TCV_{DS}		-1.6			-1.6		mV/°C	I_D = 5µA
			-0.3			-0.3		mV/°C	I_D = 50µA
			0.0			0.0		mV/°C	I_D = 68µA
			+2.7			+2.7		mV/°C	I_D = 500µA
Initial Offset Voltage [3]	V_{OSi}		1	5		1	5	mV	
Tempco of V_{OS}	TCV_{OS}		5			5		µV/°C	V_{DS1} = V_{DS2}
Differential Threshold Voltage [4]	DV_t			2.000			2.000	V	
Tempco of Differential Threshold Voltage [4]	$TCDV_t$		0.033			0.033		mV/°C	
Long Term Drift	$\Delta V_t/\Delta t$		-0.02	-0.05		-0.02	-0.05	mV	1000 Hours
Long Term Drift Match	$\Delta V_t/\Delta t$		-5			-5		µV	1000 Hours
Drain Source On Current	$I_{DS(ON)}$		3.0			3.0		mA	V_G =V_D = 5V V_S = 0V V_t = 1.0
Drain Source On Current [4]	$I_{DS(ON)}$		0.8			0.8		mA	V_G =V_D = 5V V_S = 0V V_t = 3.0
Initial Zero Tempco Voltage [3]	V_{ZTCi}		1.52			1.52		V	V_t = 1.000V
Zero Tempco Current	I_{ZTC}		68			68		µA	
Initial On-Resistance [3]	R_{ONi}		500			500		Ω	$V_{GS\,i}$= 5V V_{DS} = 0.1V
On-Resistance Match	ΔR_{ON}		0.5			0.5		%	

NOTES:
1. V+ must be the most positive supply rail and V- must be at the most negative supply rail. Source terminals other than those labeled as V- can be at any voltage between V- and V+.
2. Initial Threshold Voltage is set at the factory. If no EPAD Vt trimming is intended by user, then this is also the final or permanent threshold voltage value.
3. Initial and Final values are the same unless deliberately changed by user.
4. These parameters apply only when Vt of one or more of the devices are to be changed by user.

OPERATING ELECTRICAL CHARACTERISTICS (cont'd)
T_A = 25°C V^+ = +5.0V unless otherwise specified

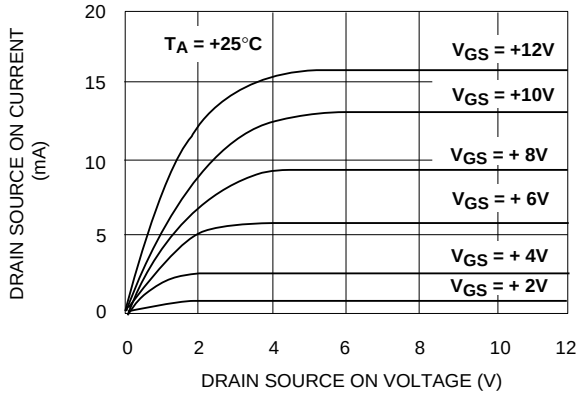
Parameter	Symbol	ALD1123E Min	ALD1123E Typ	ALD1123E Max	ALD1121E Min	ALD1121E Typ	ALD1121E Max	Unit	Test Conditions
Transconductance	gm		1.4			1.4		mA/V	V_D = 10V,V_G =V_t + 4.0
Transconductance Match	Δgm		25			25		µA/V	V_D = 10V,V_G =V_t + 4.0
Low Level Output Conductance	g_{OL}		6			6		µA/V	V_G = V_t +0.5V
High Level Output Conductance	g_{OH}		68			68		µA/V	V_G = V_t +4.0V
Drain Off Leakage Current	$I_{D(OFF)}$		5 4	400 4		5 4	400 4	pA nA	 T_A = 125°C
Gate Leakage Current	I_{GSS}		10 1	100 1		10 1	100 1	pA nA	 T_A = 125°C
Input Capacitance	C_{ISS}		25			25		pF	
Cross Talk			60			60		dB	f = 100KHz
Relaxation Time Constant [4]	t_{RLX}		2			2		Hours	
Relaxation Voltage [4]	V_{RLX}		-0.3			-0.3		%	1.0V ≤ V_t ≤ 3.0V

E-TRIM CHARACTERISTICS
T_A = 25°C V^+ = +5.0V unless otherwise specified

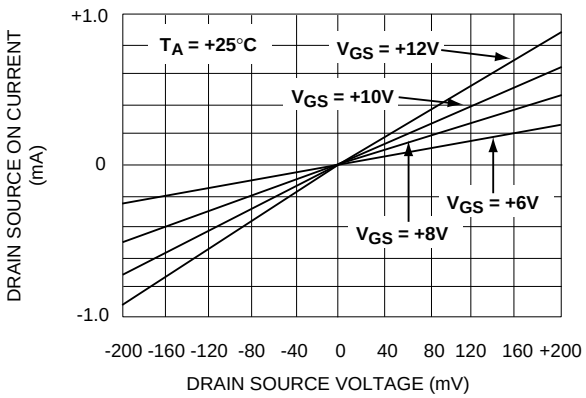
Parameter	Symbol	ALD1123E Min	ALD1123E Typ	ALD1123E Max	ALD1121E Min	ALD1121E Typ	ALD1121E Max	Unit	Test Conditions
E-trim V_t Range [4]	V_t	1.000		3.000	1.000		3.000	V	
Resolution of V_t E-trim Pulse Step [4]	RV_t		0.1	1		0.1	1	mV	
Change in V_t Per E-trim Pulse [4]	ΔV_t / N		0.5 0.05			0.5 0.05		mV/ pulse	V_t = 1.0V V_t = 2.5V
E-trim Pulse Voltage [4]	Vp	11.75	12.00	12.25	11.75	12.00	12.25	V	
E-trim Pulse Current [4]	Ip		2			2		mA	
Pulse Frequency [4]	*f* pulse		50			50		KHz	

TYPICAL PERFORMANCE CHARACTERISTICS

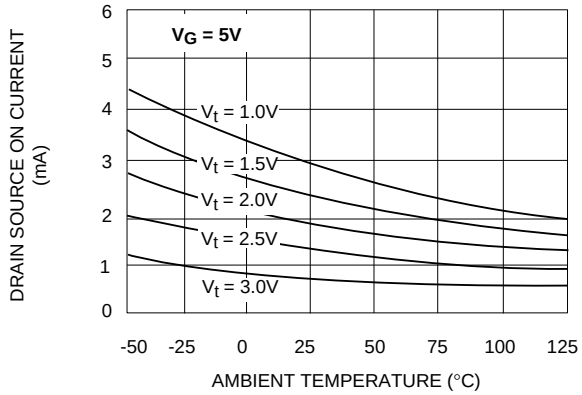
OUTPUT CHARACTERISTICS



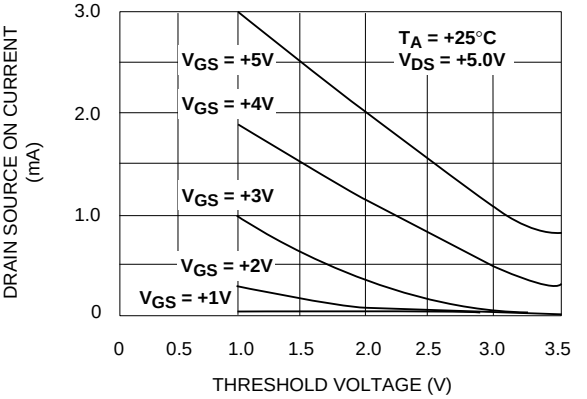
OUTPUT CHARACTERISTICS



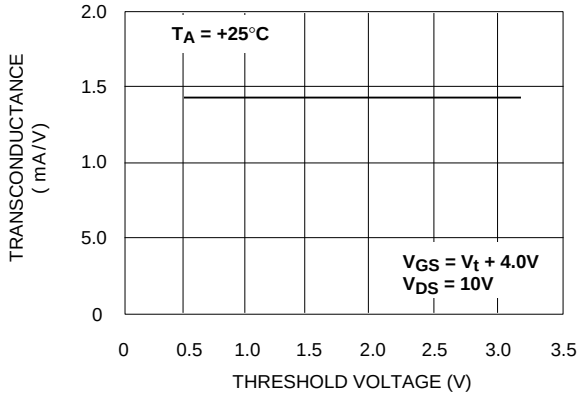
DRAIN SOURCE ON CURRENT vs. AMBIENT TEMPERATURE



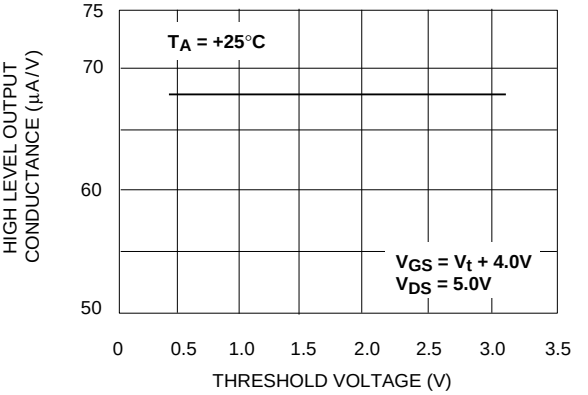
DRAIN SOURCE ON CURRENT vs. THRESHOLD VOLTAGE



TRANSCONDUCTANCE vs. THRESHOLD VOLTAGE

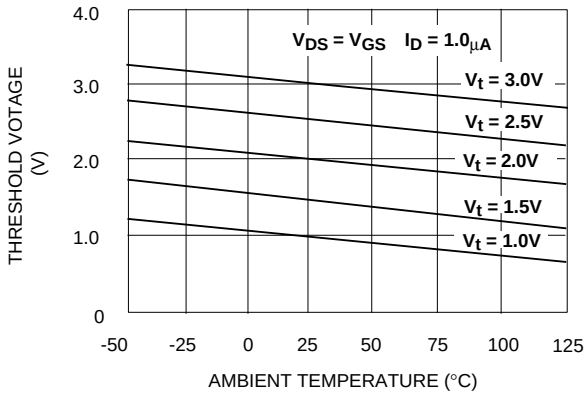


HIGH LEVEL OUTPUT CONDUCTANCE vs.THRESHOLD VOLTAGE

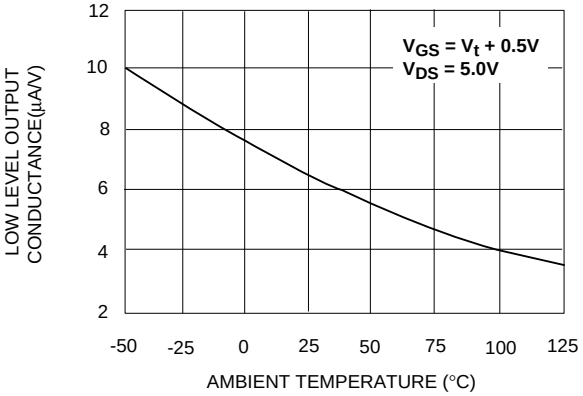


TYPICAL PERFORMANCE CHARACTERISTICS

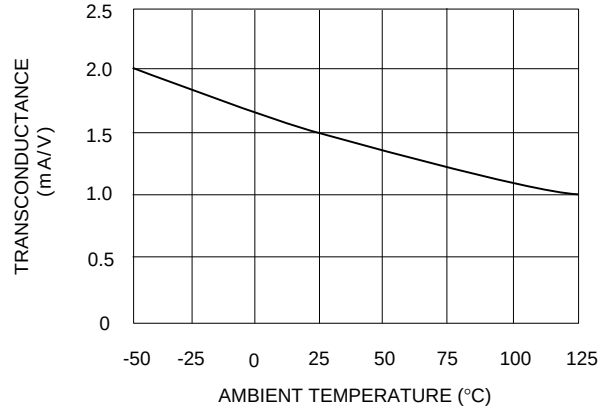
THRESHOLD VOLTAGE vs. AMBIENT TEMPERATURE



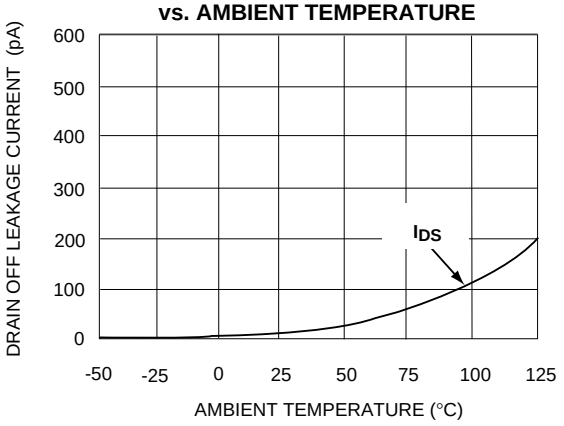
LOW LEVEL OUTPUT CONDUCTANCE vs. AMBIENT TEMPERATURE



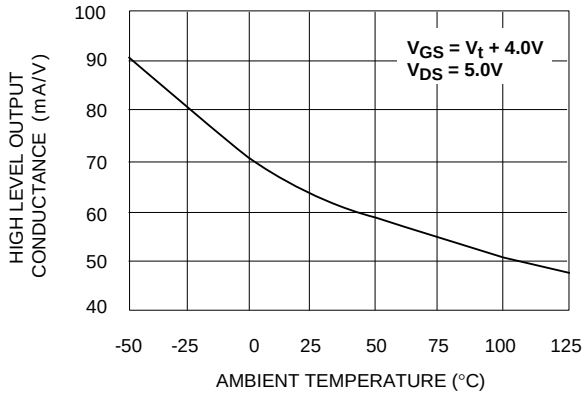
TRANSCONDUCTANCE vs. AMBIENT TEMPERATURE



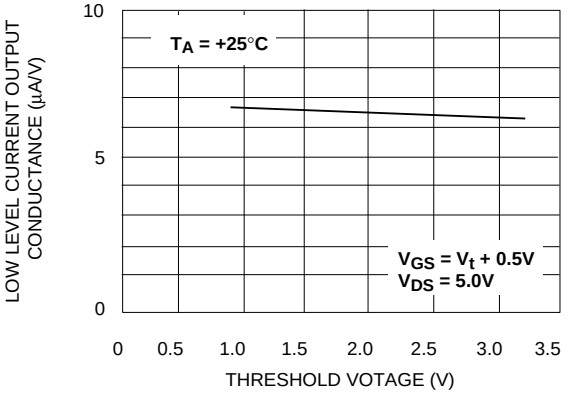
DRAIN OFF LEAKAGE CURRENT I_{DS} vs. AMBIENT TEMPERATURE



HIGH LEVEL OUTPUT CONDUCTANCE vs. AMBIENT TEMPERATURE

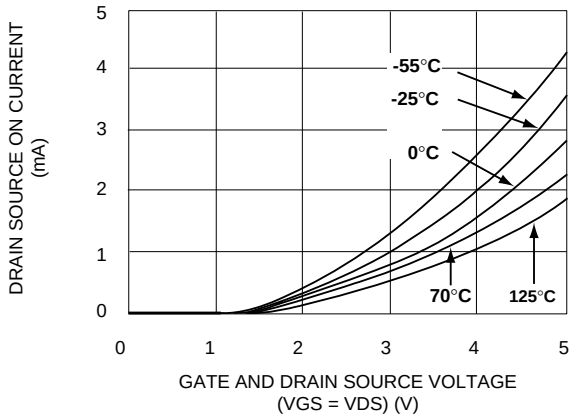


LOW LEVEL OUTPUT CONDUCTANCE vs. THRESHOLD VOLTAGE

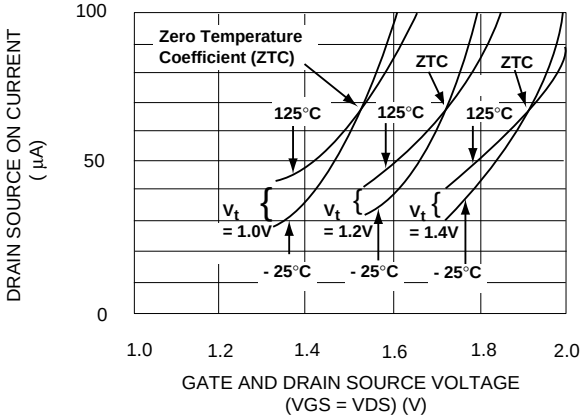


TYPICAL PERFORMANCE CHARACTERISTICS

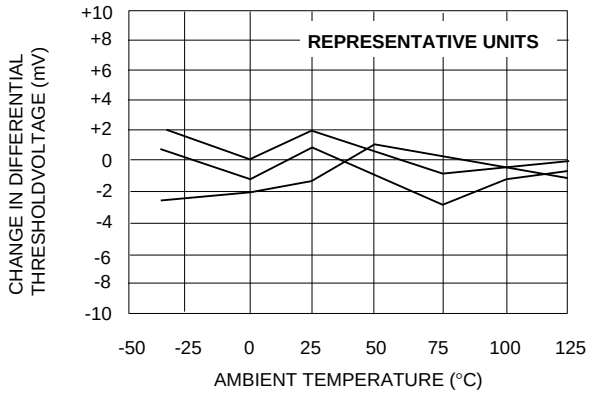
DRAIN SOURCE ON CURRENT, BIAS CURRENT vs. AMBIENT TEMPERATURE



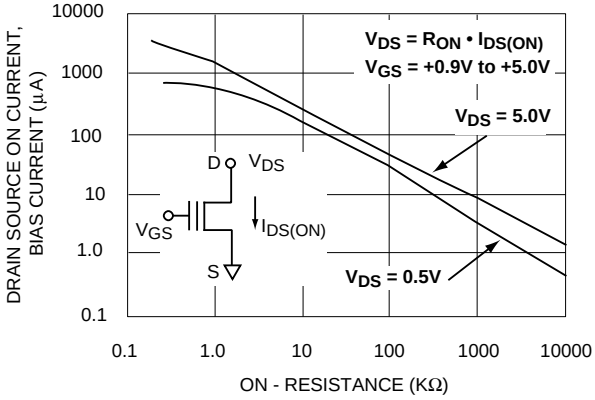
DRAIN SOURCE ON CURRENT, BIAS CURRENT vs. AMBIENT TEMPERATURE



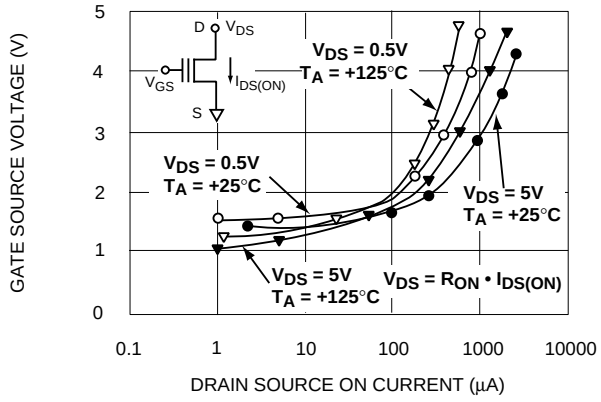
CHANGE IN DIFFERENTIAL THRESHOLD VOLTAGE vs. AMBIENT TEMPERATURE



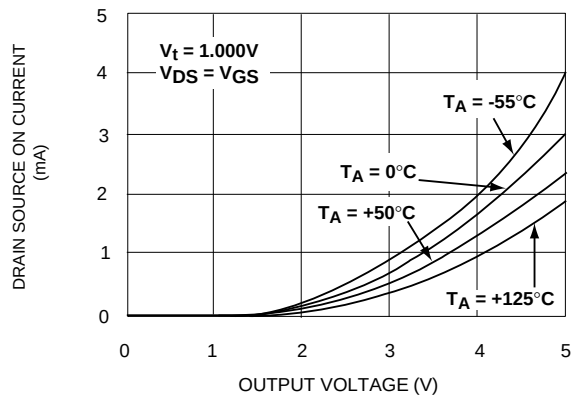
DRAIN SOURCE ON CURRENT, BIAS CURRENT vs. ON - RESISTANCE



GATE SOURCE VOLTAGE vs. DRAIN SOURCE ON CURRENT

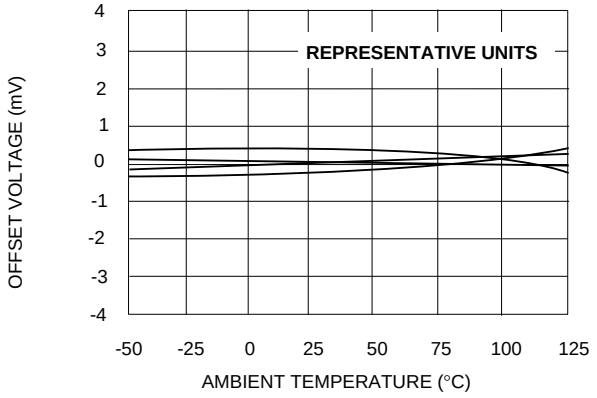


DRAIN SOURCE ON CURRENT vs. OUTPUT VOLTAGE

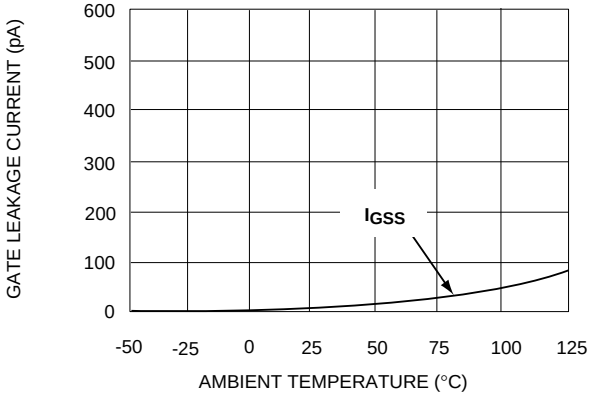


TYPICAL PERFORMANCE CHARACTERISTICS

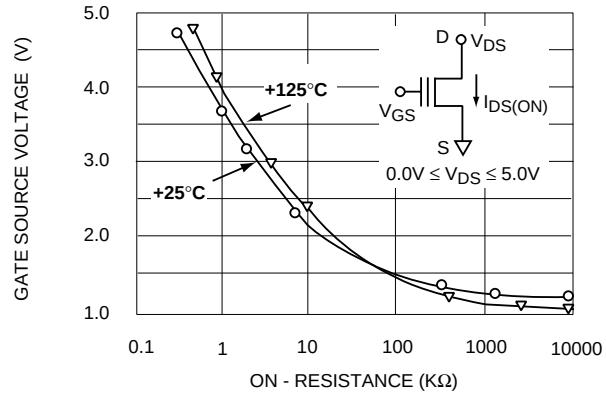
OFFSET VOLTAGE vs. AMBIENT TEMPERATURE



GATE LEAKAGE CURRENT vs. AMBIENT TEMPERATURE



GATE SOURCE VOLTAGE vs. ON - RESISTANCE



DRAIN - GATE DIODE CONNECTED VOLTAGE TEMPCO vs. DRAIN SOURCE ON CURRENT